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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/697,981	10/31/2003	Meir Avraham	246/194	8963

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EXAMINER	
SIDDIQUI, SAQIB JAVAID	
ART UNIT	**PAPER NUMBER**
2138	

DATE MAILED: 02/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/697,981	AVRAHAM, MEIR	
	Examiner	Art Unit	
	Saqib J. Siddiqui	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 January 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

The Oath filed October 31, 2003 complies with all the requirements set fort in MPEP 602 and therefore is accepted.

Drawings

The filed drawings are accepted.

Specification

The disclosure is objected to because of the following informalities:

The Applicant recites time of the "test if relatively short" (page 2, lines 7-8). The Applicant should change "if" to "is." appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made Appropriate correction is required.

Claim Objections

Claims 10 & 11 are objected to because of the following informalities:

As per claim 10:

This claim refers to "then being from the" (line 3), complicating the claim language. Applicant should omit "then being" and rewrite the claim to "from the nonvolatile memory."

As per claim 11:

This claim is objected to by virtue of its dependency.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-28 are rejected under 35 U.S.C. 102(b) as being fully anticipated by Chesley US Pat no. 4,333,142.

As per claim 1:

Chesley teaches a method of testing an electronic device that includes a CPU (Fig 2 # 22) and at least one memory (Fig 1 # 13), comprising the steps of: (a) testing the at least one memory (column 1, lines 40-42), using the CPU (column 1, lines 40-42); and b) testing the CPU (column 1, lines 42-44).

As per claim 2:

Chesley teaches the method wherein said testing of the CPU is effected subsequent to said testing of the at least one memory (column 3, lines 37-39).

As per claim 3:

Chesley teaches the method further comprising the step of: (c) loading a testing program into one of said at least one memory (Fig 3, # 27, column 3, lines 1-2), the CPU then testing at least one of said at least one memory by executing said testing program (column 3, lines 2-6).

As per claim 4:

Chesley teaches the method further comprising the step of: (c) storing results of said testing of said at least one memory in one of said at least one memory, by the CPU (Fig 3 # 24, column 3, lines 5-9).

As per claim 5:

Chesley teaches the method; wherein said testing of the CPU includes reading said stored results from said one of said at least one memory (column 3, lines 37-39).

As per claim 7:

Chesley teaches a method of testing an electronic device that includes a CPU (Fig 2 # 22), a nonvolatile memory (Fig 1 # 13) and a volatile memory (Fig 1 # 14), comprising the steps of: (a) testing at least one of the memories (column 1, lines 40-42), using the CPU (column 1, lines 40-42); and b) testing the CPU (column 1, lines 42-44).

As per claim 8:

Chesley teaches the method wherein said testing of the CPU is effected subsequent to said testing of the at least one memory (column 3, lines 37-39).

As per claim 9:

Chesley teaches the method, further comprising the step of: (c) loading a testing program into the volatile memory, the CPU then testing at least one of the memories by executing said testing program (column 3, lines 47-49).

As per claim 10:

Chesley teaches the method further comprising the step of: (d) storing said testing program in the nonvolatile memory (column 3, lines 7-10), said loading of the testing program into the volatile memory then being from the nonvolatile memory (column 3, lines 47-49).

As per claim 11:

Chesley teaches the method wherein said loading of the testing program from the nonvolatile memory to the volatile memory is effected by the CPU (column 3, lines 47-49).

As per claim 12:

Chesley teaches the method further comprising the step of: (c) storing results of said testing in the nonvolatile memory, by the CPU (Figure 2 # 28, column 3, lines 49-54).

As per claim 13:

Chesley teaches the method wherein said testing of the CPU includes reading said stored results from said nonvolatile memory (column 3, lines 55-60).

As per claim 14:

Chesley teaches the method further comprising the step of: (c) storing a testing program in the nonvolatile memory (column 3, lines 7-10), the CPU then testing at least one of the memories by executing said testing program directly in said nonvolatile memory (column 3, lines 10-16).

As per claim 15:

Chesley teaches the method of claim 14, further comprising the step of: (d) storing results of said testing in the nonvolatile memory, by the CPU (column 3, lines 30-37).

As per claim 16:

Chesley teaches the method, wherein said testing of the CPU includes reading said stored results from said nonvolatile memory (column 3, lines 37-46).

As per claim 18:

Chesley teaches a method of testing a nonvolatile memory that is included in a system-in-package, comprising the steps of: (a) including a CPU in the system-in-package (Fig 2 # 22); (b) storing a testing program in the nonvolatile memory (column 3, lines 7-10); and (c) executing said testing program, by said CPU, in order to test the nonvolatile memory (column 3, lines 10-16).

As per claim 19:

Chesley teaches the method, further comprising the step-of: (d) loading said testing program from the nonvolatile memory into a volatile memory, said executing of said testing program then being from said volatile memory (column 3, lines 46-49).

As per claim 20:

Chesley teaches the method further comprising the step of: (e) including said volatile memory in the system-in-package (Fig 1 #14).

As per claim 21:

Chesley teaches the method, further comprising the step of: (d) storing results of said executing in the nonvolatile memory (Figure 2 # 28, column 3, lines 49-54).

As per claim 23:

Chesley teaches an electronic device comprising: (a) a nonvolatile memory (Fig 1 # 13), wherein is stored a first testing program for testing said nonvolatile memory (column 3, lines 7-10); and (b) a volatile memory (Fig 1 # 14), operationally connected to said nonvolatile memory (Fig 1 # 24); and wherein a second program, for testing said volatile memory, is stored in said nonvolatile memory (column 3, lines 47-49).

As per claim 24:

Chesley teaches the electronic device wherein said nonvolatile memory and said volatile memory are fabricated as separate respective chips (Fig 1 #13 & # 14) and are packaged together in a common package (Fig 1 # 11).

As per claim 25:

Chesley teaches the electronic device further comprising: (c) a CPU (Fig 2 # 22), fabricated on a respective chip (Fig 1 # 12), and operationally connected to at least one of said nonvolatile memory (Fig 1 # 27) and said volatile memory (Fig 1 # 26); said CPU being packaged together with said memories in said common package (Fig 1 # 11).

As per claim 26;

Chesley teaches a method of testing a system-in-package that includes a nonvolatile memory (Fig 1 # 13) and a volatile memory (Fig 1 # 14), comprising the steps of: (a) executing a first testing program in order to test the volatile memory (column 3, lines 47-49); and (b) storing results of said executing in the nonvolatile memory (column 3, lines 49-53).

As per claim 27:

Chesley teaches the method further comprising the steps of: (c) executing a second testing program in order to test the nonvolatile memory (column 3, lines 10-16); and (d) storing results of said executing of said second testing program in the nonvolatile memory (column 3, lines 30-45).

Claim Rejections - 35 USC § 103

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 6, 17, 22 & 28 are rejected under 35 U.S.C. 103(a) as being unpatentable Chesley US Pat no. 4,333,142, and further in view of Takizawa US Pat no. 6198663 B1

As per claim 6:

Chesley substantially teaches a method of testing an electronic device that includes a CPU (Fig 2 # 22) and at least one memory (Fig 1 # 13), comprising the steps of: (a) testing the at least one memory (column 1, lines 40-42), using the CPU (column 1, lines 40-42); and b) testing the CPU (column 1, lines 42-44).

Chesley does not explicitly teach teaches the method, wherein said testing of said at least one memory is effected during a burn-in of the electronic device.

However, Takizawa in an analogous art teaches the method, wherein said testing of said at least one memory is effected during a burn-in of the electronic device (Figure 1 # 61a, column 4, lines 34-47). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to execute testing during a burn-in of the electronic device, since one of ordinary skill in the art would have recognized that executing testing during a burn-in would have assisted in stabilizing

outputs, and identifying early life failures normally resulting from thermal or other effects.

As per claims 17, 22 & 28:

Rejected based on the same argument as claim 6.

Related Art

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Additional pertinent prior arts, US Pat no. 6151692, US Pat no. 6009539 A, US Pat no. 5566303 A, US Pat no. 5525971 A, US Pat no. 6832348 B2 mention the same self-testing procedure of a memory using a CPU and both non-volatile and volatile memories are included herein for Applicant's review.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saqib J. Siddiqui whose telephone number is (571) 272-6553. The examiner can normally be reached on 8:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SS

Saqib Siddiqui
Art Unit 2138
01/27/2006

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